Microwave Noise in Semiconductor Devices

Module 4

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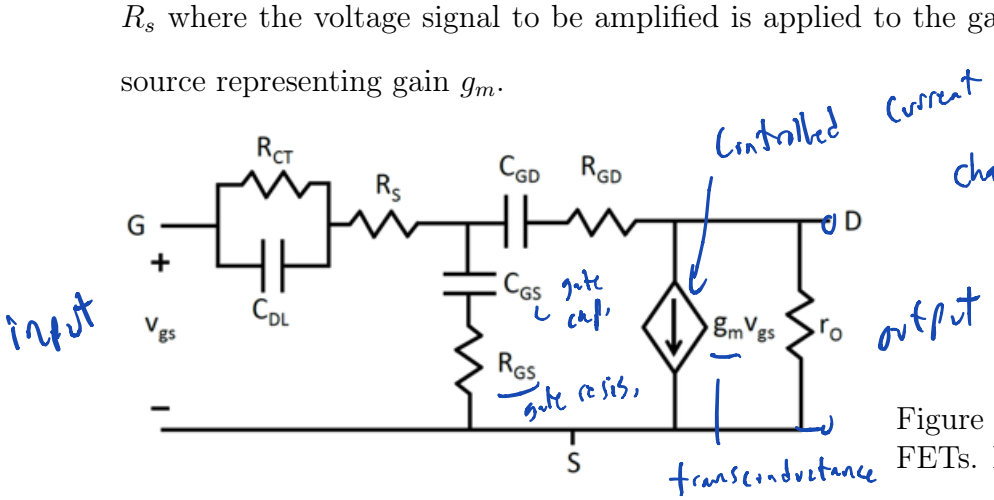
HBTs

1 Equivalent circuit models of noise in HEMTs and BJTs

Now that we know the microscopic origin of the basic noise sources in electronic devices and how to place them into linear electrical networks, we can examine the effects of noise in HEMTs and BJTs/HBTs. First, we need to write down the equivalent circuits for transistors; we will then figure out how to include the noise sources.

1.1 Equivalent circuit model of noiseless FET

Below is a small-signal model for a field-effect transistor. Key features are a source resistnce R_s where the voltage signal to be amplified is applied to the gate and a controlled current source representing gain g_m.



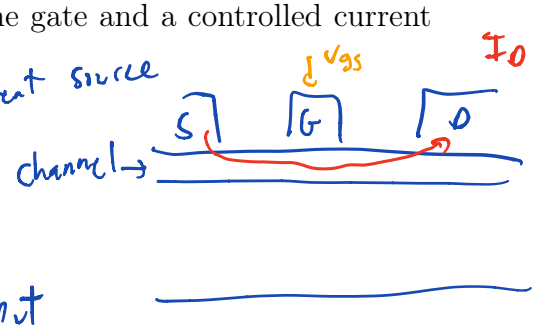


Figure 1: Small signal model for FETs. https://www.mdpi.com.

1.2 Noise in HEMTs - Pospieszalski model

1.2.1 History

Some history [history of hot electron noise discussed in a later module]

- 1960s Lax, Kogan, others - mathematical foundations of random processes and electronic noise.

- 1960: Price's theory of intervalley noise, the first mention of it.
- 1962: Shockley et al discuss various physical mechanisms for noise in semiconductors including intervalley scattering.
- 1962-5: van der Ziel analyzes the noise arising from the finite resistance of a channel in a field effect transistor. They consider that noise fluctuations in the channel couple capacitively to create noise currents in the gate (note the cause and effect here).
- 1970-1972 - Baechtold attributes "drain noise" to intervalley scattering, citing Shockley (this is what we believe is the correct explanation). The noise can be thought of as a type of GR noise, also referred to as partition noise.
- 1975 - Pucel describes a theory of noise of a FET and equivalent circuit model that include 3 adjustable parameters based on van der Ziel's work. It is used for JFETs.
- 1976 - Frey studies noise from intervalley scattering using Monte Carlo simulations.
- 1979 - Fukui introduces empirical model for noise temperature versus frequency.
- 1980: Weinreb reports measurements of the noise properties of GaAs FET amplifiers down to cryogenic temperatures.
- Early 1980s: hot electron transport studied using computer simulations (MC).
- 1985: Gasquet et al - experiments investigating role of intervalley scattering on noise in n+ n n+ Gunn diodes of GaAs.
- 1986: Brookes - Pucel theory applied to HEMTs.
- 1987-88: Stanton and Wilkins solve two-band BTE to study intervalley scattering.
- 1987-88: Gupta et al report a one-parameter noise model for noise at room temperature.

In 1989, Pospeczialski introduces his now widely used noise model for FETs. The key idea is that two noise generators exist, one at the gate and one at the drain. Unlike previous works, the gate noise generator is postulated to arise from voltage fluctuations in the gate (thermal) that alter the drain current (not the other way around as in van der Ziel!) The relevant noise temperature of the gate is postulated to be the physical temperature of the device and thus has physical meaning.

The drain temperature is found to be $\sim$ 1000s of K, a value that is consistent with intervalley scattering (cf Gasquet et al).

The evidence for this perspective, as discussed on p1348 of Posp, is that the gate noise temperature does in fact decrease with physical temperature (and appears to be equal to the physical temperature) while drain noise temp does not. In contrast, the van der Ziel picture should have the drain and gate noise temps decrease in a similar way.

Here's how the model works. Recall that there are different ways to represent a noisy two-port: The first (a) is best for the admittance representation, and the second (b) is natural for the ABCD representation.

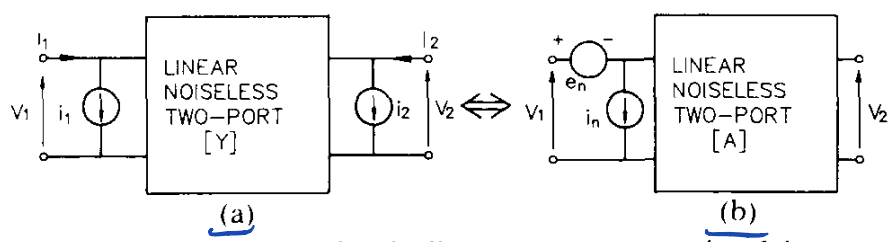


Fig. 1. Noise representation in linear two-ports: (a) involving current noise sources at the input and output and (b) involving current and voltage noise source at the input.

Figure 2:

In each representation, we can define various noise parameters. Admittance:

$$G_1 = \frac{\overline{|i_1|^2}}{4k_B T_0 \Delta f} \qquad G_2 = \frac{\overline{|i_2|^2}}{4k_B T_0 \Delta f}$$

$$\rho_c \equiv \frac{\overline{i_1^* i_2}}{\sqrt{\overline{|i_1|^2}\,\overline{|i_2|^2}}}$$

ABCD:

$$R_n = \frac{\overline{|e_n|^2}}{4k_B T_0 \Delta f} \qquad g_n = \frac{\overline{|i_n|^2}}{4k_B T_0 \Delta f}$$

$$\rho = \frac{\overline{e_n^* i_n}}{\sqrt{\overline{|e_n|^2}\,\overline{|i_n|^2}}}$$

Another representation based on minimum noise temperature:

$$T_n = T_{min} + 4NT_0 \frac{|\Gamma_g - \Gamma_{opt}|^2}{(1-|\Gamma_g|^2)(1-|\Gamma_{opt}|^2)}$$

$$N = R_{opt}\, g_n$$

$$\Gamma_{opt} = \frac{Z_{opt} - Z_0}{Z_{opt} + Z_0}$$

$$M = \frac{T_n}{T_g} \quad \frac{1}{1 - G_a} \leftarrow \text{available gain}$$

A physical constraint exists:

$$\rightarrow T_{min} \leq 4NT_0$$

Here is the proposed noise equivalent circuit, including parasitics:

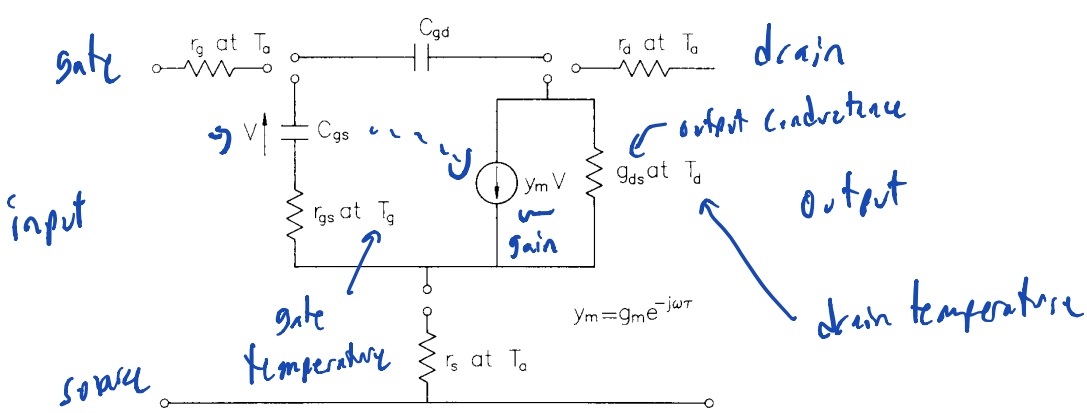


Fig. 2. Equivalent circuit of FET (HEMT, MODFET) chip. Noise properties of an intrinsic chip are represented by equivalent temperatures: T_g of r_{gs}, and T_d of g_{ds}. Noise contribution of ohmic resistances r_s, r_g, and r_d are determined by physical temperature T_a of a chip. The process of de-embedding is illustrated by unconnected elements (compare Table I).

Figure 3:

And here is the circuit we will use for analysis, for an intrinsic chip:

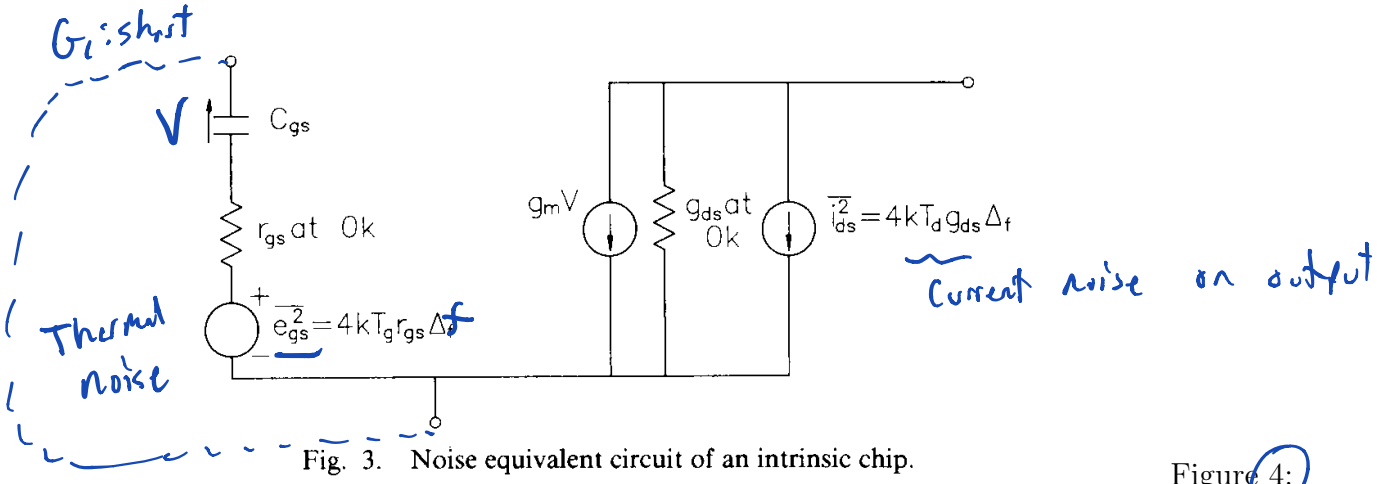


Fig. 3. Noise equivalent circuit of an intrinsic chip.

Figure 4:

From this circuit, we can derive the noise parameters in admittance rep:

G_1: $Y_1 = \dfrac{1}{r_{gs} + \frac{1}{j\omega C_{gs}}} \cdot e_{gs}$

$$G_1 = \frac{|i_1|^2}{4k_B T_0 \Delta f} = \frac{T_g}{T_0} \frac{r_{gs}\omega^2 C_{gs}^2}{1 + (r_{gs}\omega C)^2}$$

$$\overline{i_1^2} = \frac{4k_B T_g r_{gs} \Delta f}{r_{gs}^2 + \frac{1}{\omega^2 C_{gs}^2}}$$

$$G_2 = \frac{T_g}{T_0} \frac{g_m^2 r_{gs}}{1 + (\omega C_{gs} r_{gs})^2} + \frac{T_d}{T_0} \cdot g_{ds}$$

$$c_{01} = \rho_c \sqrt{G_1 G_2}$$

We observe that if $T_d = 0$, $\rho_c = -j \cdot 1$. So the noise voltage source $\overline{e_{gs}^2}$ models a noise process yielding perfectly correlated noise currents in drain and gate.

Physically, we interpret it as voltage fluctuations in the gate modulating the drain current.

The current noise source $\overline{i_{ds}^2}$ models a noise process that is only in the drain.

For completeness, we can express these noise parameters in the other representations.

Optimum noise parameter:

Optimum source impedance

$$X_{opt} = \frac{1}{\omega C_{gs}} \tag{1}$$

$$R_{opt} = \sqrt{\left(\frac{f_T}{f}\right)^2 \frac{r_{gs}}{g_{ds}} \frac{T_g}{T_d} + r_{gs}^2} \tag{2}$$

$$T_{min} = 2\frac{f}{f_T}\sqrt{g_{ds} r_{gs} T_g T_d + \left(\frac{f}{f_T}\right)^2 r_{gs}^2 g_{ds}^2 T_d^2} + 2\left(\frac{f}{f_T}\right)^2 r_{gs} g_{ds} T_d \tag{3}$$

$$g_n = \left(\frac{f}{f_T}\right)^2 \frac{g_{ds} T_d}{T_0} \tag{4}$$

$$\frac{4NT_0}{T_{min}} = \frac{2}{1 + \frac{r_{gs}}{R_{opt}}} \tag{5}$$

$$R_n = \frac{T_g}{T_0} r_{gs} + \frac{T_d}{T_0} \frac{g_{ds}}{g_m^2}(1 + \omega^2 C_{gs}^2 r_{gs}^2) \tag{6}$$

$$cor = \rho\sqrt{R_n g_n} = \frac{T_d}{T_0} \frac{g_{ds}}{g_m^2}(\omega^2 C_{gs}^2 r_{gs} + j\omega C_{gs}) \tag{7}$$

$$f_T = \frac{g_m}{2\pi C_{gs}} \tag{8}$$

The available gain for a given generator impedance is:

$$G_{a,max} = \left(\frac{f_T}{f}\right)^2 \frac{1}{4 g_{ds} r_{gs}} \tag{9}$$

$$g_g = \left(\frac{f}{f_T}\right)^2 g_{ds} \tag{10}$$

$$Z_{opt}^G = r_{gs} + j\frac{1}{\omega c_{gs}} \tag{11}$$

$$X_{opt}^M = X_{opt}^G = X_{opt} = \frac{j}{\omega C_{gs}} \tag{12}$$

Finally, we can find the generator impedance that minimizes noise:

$$R_{opt}^M = r_{gs}\left[\sqrt{\left(\frac{T_g}{T_d}-1\right)^2+\frac{R_{opt}^2}{r_{gs}^2}-1}-\frac{T_g}{T_d}\right] \tag{13}$$

$$= r_{gs}\left[\sqrt{\left(\frac{T_g}{T_d}-1\right)^2+4G_{a,max}\frac{T_g}{T_d}}-\frac{T_g}{T_d}\right] \tag{14}$$

1.3 Approximate expressions

The above equations are given for completeness. To get physical insight, consider a few limits.

Case 1: low frequency

If $\frac{f}{f_T} \ll \sqrt{\frac{T_g}{T_d}\frac{1}{r_{gs}g_{ds}}}$

then $R_{opt} \gg r_{gs}$ so that we have

$$R_{opt} \simeq \frac{f_T}{f}\sqrt{\frac{r_{gs}T_g}{g_{ds}T_d}} \qquad T_{min} \simeq 2\frac{f}{f_T}\sqrt{g_{ds}T_d r_{gs}T_g}$$

Some observations:

cutoff frequency

1. Minimum noise temperature increases linearly with f/f_T → as high f_T as possible is desired.

2. Minimum noise temperature depends on ambient temperature due to gate resistance → operate cold for best noise performance. (thermal noise gen),

3. The drain temperature matters and is known to be $\gg T_g$ → we need to better understand the origin of drain noise. $T_d \sim 10^3$ K

A related useful result is

$$\frac{4NT_0}{T_{min}} = \frac{4R_{opt}g_nT_0}{T_{min}} = 2\ !$$

Case 2 $T_g \to 0$

In this case we only have an uncorrelated drain noise current source. We find

$$R_{opt} \simeq r_{gs} \qquad T_{min} \simeq 4\left(\frac{f}{f_T}\right)^2 r_{gs}\, g_d\, T_d$$

drain temp

A related result is

$$\frac{4NT_0}{T_{min}} \simeq 1$$

Posp then argues that if the model describes the noise parameters of a physical FET, we must have

$$1 \leq \frac{4NT_0}{T_{min}} \leq 2$$

The LHS inequality follows from the physicality of the two-port, while the RHS one follows from the model (as $R_{opt} \to \infty$, we see at the bottom of p6 the stated result).

After this, Posp shows that the model agrees well with the measurements ~~for~~ if T_g around the physical temperature and T_d on the order of 10^3 of K. The latter value is consistent with noise measurements done on HEMT structures lacking a gate (see 10.1109/T-ED.1987.23344).

He also discusses that assigning the temperature of the gate noise generator as the physical temperature is not necessarily obvious. Many effects can be modeled with a voltage noise generator in series with a depletion layer capacitance, e.g. random variation in depletion layer density. Figuring out the answer is made harder by the difficulty of determining r_{gs}. But, variable temperature measurements show that cooling

leads to decreases in the best fit value of T_g, suggesting the origin of the noise generator is thermal in origin.

This way of thinking about the gate noise is qualitatively different from the previous works, e.g. Pucel. In those works, the gate noise current was thought of as induced by drain current fluctuations. But that predicts that both T_d & T_g should decrease on cooling in the same way, which is not observed.

T_g ~ physical temp

T_d ~ indep. of T

1.4 Illustrative data

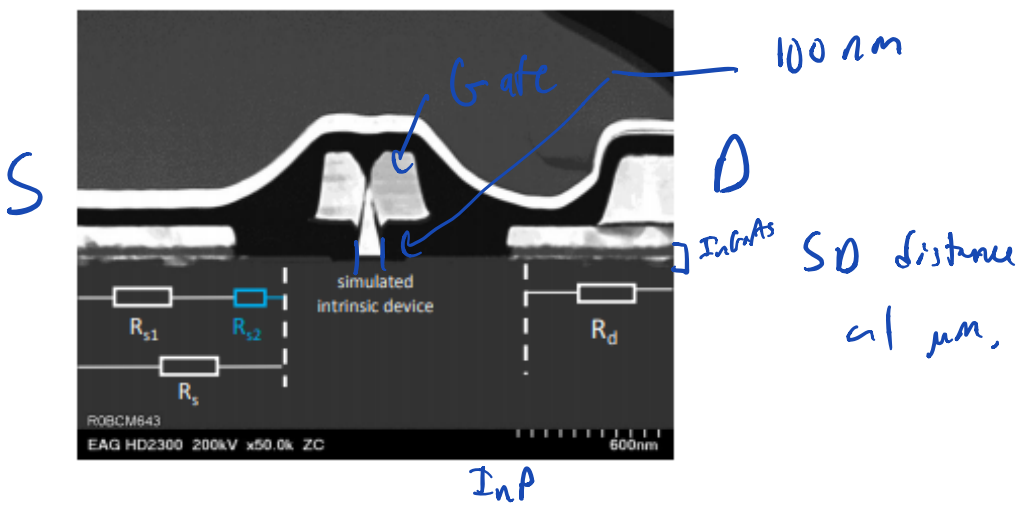


Figure 5: STEM image of InP-HEMT showing separation between the intrinsic device and external resistances. From Joel Schleeh's thesis

Let's now see how these models can be used. Here is an example of what you measure in a microwave noise characterization setup - gain and noise temperature.

These measurements, plus additional measurements of e.g. S parameters, allow you to construct a small signal model of the device at a particular bias point (V_{DS}), physical temperature, T and other conditions. This model then allows you to extract the drain temperature which is constant (indep. of f) in the typical frequency bands of interest. Since in the Posp model the noise generators arise from gate and drain temperatures plus the corresponding resistances, knowledge of these parameters allows one to understand the relative importance of the different noise mechanisms and effect of varying parameters.

As an example, here is a figure of the minimum noise temperature as drain current is varied.

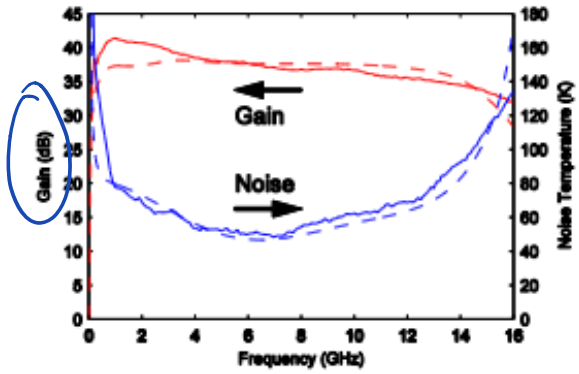


Figure 6: Measured (solid) and simulated (dashed) gain and noise temperature of a 0.5-13 GHz LNA module at 300 K, $V_d = 2.35$ V and $I_d = 45mA$. From Joel Schleeh's thesis

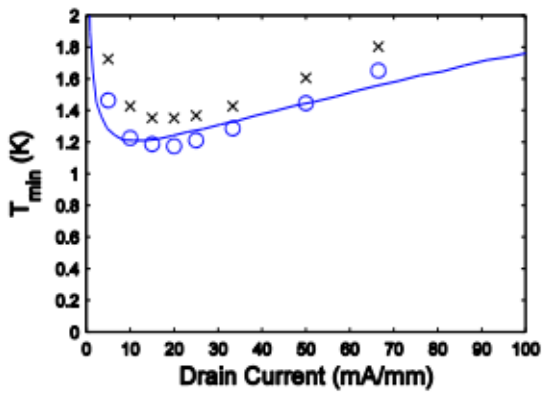


Figure 7: Extracted T_{min} at 6 GHz and 10 K (markers) and simulated results from extracted $f_T, R_t, G_{ds}, T_{drain}$ (solid). From Joel Schleeh's thesis

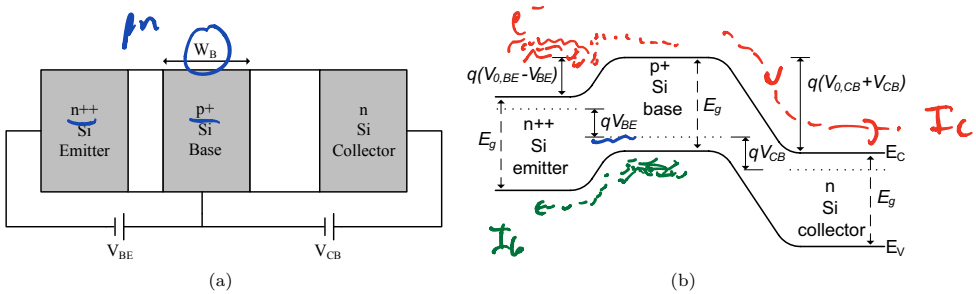
These models can also aid in designing new amplifiers by enabling some level of optimization before laboratory work starts.

2 BJTs and HBTs

[Joe Bardin's thesis]

2.1 Physical layout

Recall that a BJT consists of two pn junctions back to back, usually in npn configuration.



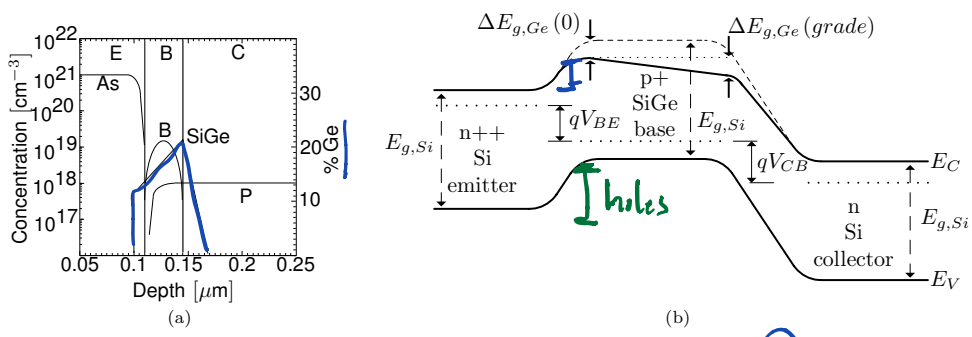
$W_B \ll L_B$ = minority carrier diffusion length

Figure 2.1: (a) Basic BJT structure. The white areas indicate the base–emitter and base–collector depletion regions. (b) Energy-band-diagram for a standard bipolar transistor under forward active bias. The Fermi levels are indicated by dotted lines in each region and would line up under zero bias. Note that the bandgap, E_g, is the same in all regions of the device.

Figure 8:

A voltage V_{BE} is applied to the first ~~configuration~~ junction, injecting electrons across the emitter-base potential barrier. Holes are also injected from the base to the emitter, comprising part of the base current (the rest is recombination of electrons in the base).

Most electrons drift across the base to the collector and form the collector current I_c that is the output of the amplifier. So we see we have a transconductance: a small rf voltage can turn into a big current I_c.



Current gain $\beta = \frac{I_c}{I_b}$

Figure 2.2: (a) A typical doping and Ge profile for a state-of-the-art SiGe HBT [59]. (b) Band Diagram for a SiGe HBT indicating deviation from that of a pure silicon transistor. Apparent bandgap narrowing effects that are discussed below have not been included in the band diagram.

Figure 9:

An HBT is just a BJT with a smaller bandgap base material (like SiGe). In that way the undesirable tradeoff between base resistance and current gain can be broken. The concept of an HBT was proposed in 1957 by Kroemer, and only in the 1990s were competitive devices realized.

2.2 Small signal model

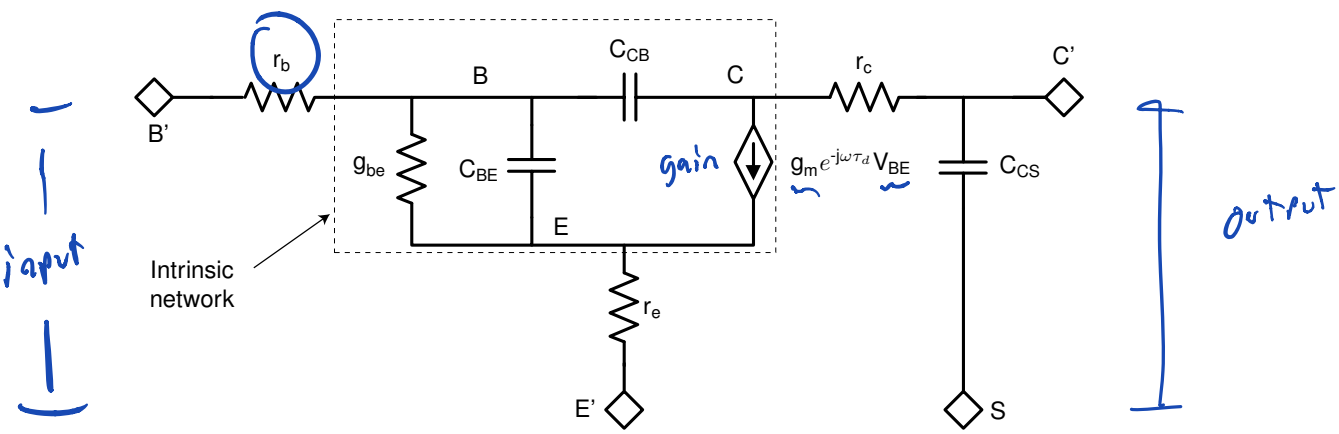


Figure 2.4: Small-signal equivalent circuit for SiGe HBT

Figure 10:

Similar to the FET/HEMT case, the small-signal circuit model can be expressed using a voltage-controlled current source.

2.3 Noise model

There are similarities and differences with the FET noise sources. Like the FET, any resistance has a spectral noise power associated with it. For HBTs, the dominant thermal noise is from the base resistance.

Unlike the FET, with the HBT shot noise occurs due to emission of electrons and holes over the BE potential barrier. Therefore, we need 2 shot noise generators.

electrons injected into base
holes " " emitter

Here is the equivalent noise circuit:

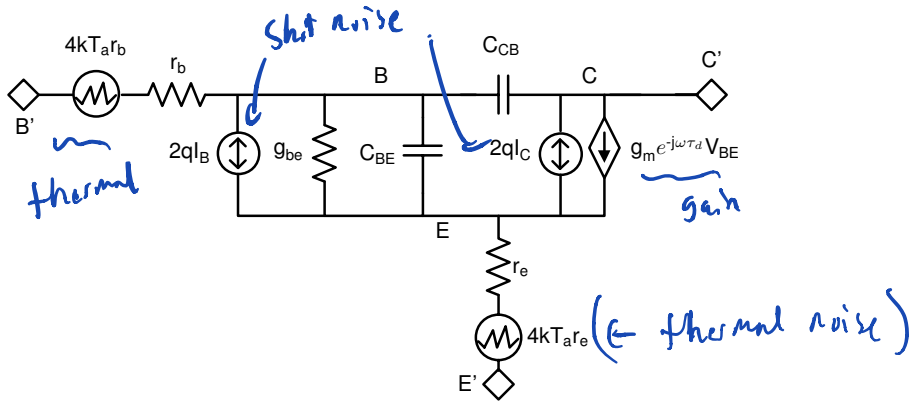
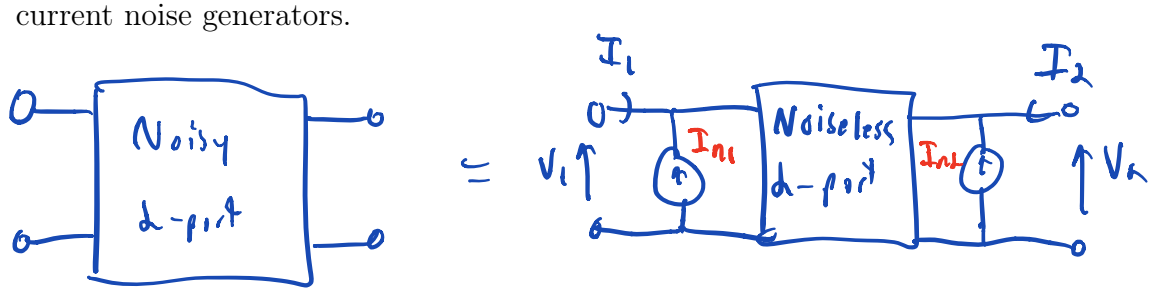


Figure 2.6: Simplified SiGe HBT noise model. The effects of the collector resistance and collector–substrate capacitance have been ignored

Figure 11:

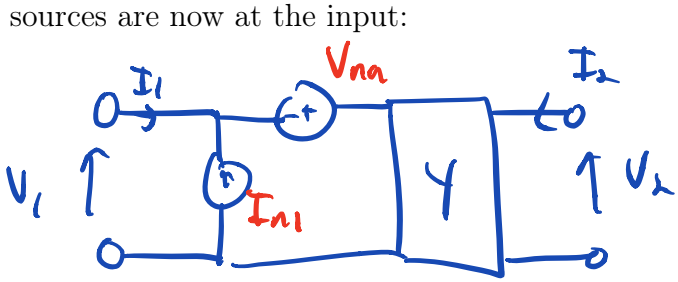
We can make progress on understanding noise in this equivalent circuit as follows. [Cressler and Niu, p265] Consider a noisy two port as a noiseless network with two external parallel current noise generators.



We can describe it mathematically in the admittance representation as:

$$\begin{pmatrix} I_1 + I_{n1} \\ I_2 + I_{n2} \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix}$$

It is generally convenient to refer back to input using the chain representation. The noise sources are now at the input:



The IV relations are

$$\begin{pmatrix} I_1 + I_{nn} \\ I_2 \end{pmatrix} = [y] \begin{pmatrix} V_1 + V_{nn} \\ V_2 \end{pmatrix}$$

so that we can link the noise generators in each representation:

Now we can account for shot noise in the base and collector currents as:

from which we get the spectral densities:

Finally, we can add in thermal noise from the base resistance since it is uncorrelated with shot noise. The spectral density of voltage fluctuations becomes

Summarizing, we have the spectral densities and the cross-correlation as:

$$S_{i_n} = 2q\frac{I_c}{\beta} + \frac{2qI_C}{|\frac{Y_{21}}{Y_{11}}|^2} \tag{15}$$

$$S_{v_n} = 4k_BTr_B + \frac{2qI_C}{|Y_{21}|^2} \tag{16}$$

$$S_{i_n v_n^*} = \frac{2qI_C Y_{11}}{|Y_{21}|^2} \tag{17}$$

So, if we had the Y parameters we could get expressions for the spectral densities of noise and hence noise figure, optimum source resistance, and so on.

Consider the following simplified circuit to get the Y parameters:

You can obtain the Y parameters in the usual way by considering voltages and currents as various terminals are left open or shorted. The result is:

The current gain cutoff frequency is known from analysis of the original circuit as $f_T = g_m/2\pi C_i$ where $C_i = C_{be} + C_{bc}$.

With these parameters, we can get the spectral densities of noise:

Now, we will use results from the optimum parameter representation of 2-ports to link these spectral densities to figures of merit of the device. The equations are long so I will give an approximate expression for the noise figure:

2.4 Optimizing an HBT

We can now use these insights to understand how design choices impact the noise figure of an HBT.

2.4.1 Emitter width scaling at fixed current density

The emitter width is the lateral dimension for a side-view perspective of an HBT. Say we scale it by M. Then g_m and r_b both scale by M since $g_m \propto I_C$ and r_b depends on the distance to the base contact.

We see that NF_{min} changes to:

Taking $0 < M < 1$, we see that . So a smaller emitter width decreases the noise.

2.4.2 Emitter length scaling at fixed current density

The emitter length is the dimension into the page. Say we scale it by N. The base resistance decreases by N. g_m and all capacitances increase by N. So no change in noise occurs. The emitter length is instead chosen to minimize the total current I_C and thereby minimize power dissipation, and also to ensure that the optimum source impedance is 50 Ω.

2.5 Illustrative data

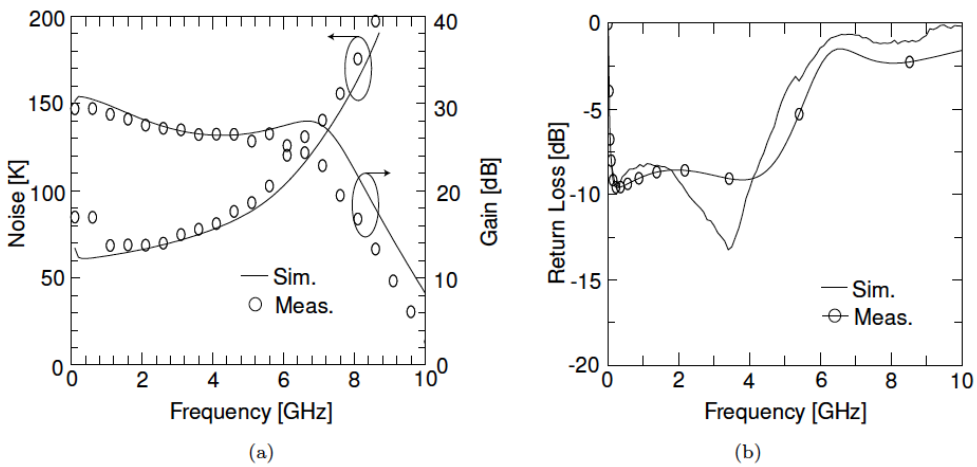


Figure 12: Noise temperature, gain and return loss data for a SiGe HBT LNA at 300K physical temperature. *(obtained from Joseph Bardin's thesis)*

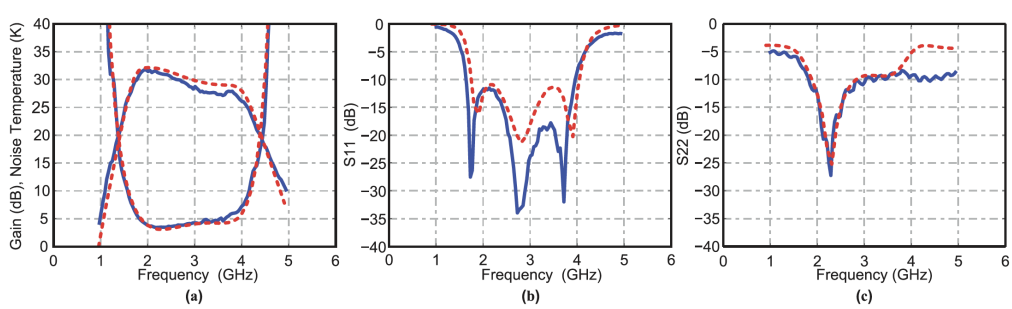


Figure 13: Noise temperature and S-parameter data for a low-power 2-4GHz SiGe HBT LNA at 15K physical temperature. The simulated data (red dashed lines) is calculated using a small-signal model and agrees well with measured data (blue lines). *(obtained from Montazeri et al, 2016)*

As in the case with HEMTs, small-signal models of HBTs, like the one discussed earlier, help characterize and optimize the performance of physical devices. The figures below depict quantitative results of a typical SiGe HBT LNA characterization; noise temperature, gain and return losses. Using simple measurements like S-parameter data, it is possible to extract a model for certain operating conditions. These models are verified by comparing measured and simulated quantities as show in the plots. Fitting these measurements to a detailed model allows us to gain insight into the physics of the device, as well as predict other relevant quantities. More importantly, having an accurate model provides tuning knobs to understand which quantities ($g_m, R_b, C_{cb}, etc.$) primarily contribute to noise and amplification performance. Finally, tuning these parameters in the model to achieve optimal performance (e.g. minimum noise temperature T_{min}) is vital in influencing future iterations of HBT fabrication and development.